

Patent

Customer No.: 31561
Docket No. 11314-US-PA
Application No.: 10/605,661**RECEIVED**
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Applicant : Lai
Application No. : 10/605,661
Filed : 2003/10/16
For : THIN FILM TRANSISTOR AND PIXEL STRUCTURE
THEREOF
Art Unit : 2815
Examiner : LEE, EUGENE

TRANSMITTAL LETTER

002-1-703-872-9306

(Via fax: 1+6 pages)

Assistant Commissioner for Patents
Arlington, Virginia 22202

Dear Sir,

In response to the Office Action dated December 10, 2004 (paper No. 20041202), please find the *Amendment and Response to Restriction Requirement* in 6 pages.

I believe that no fee is incurred. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.: 11314-US-PA)

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property OfficeDate: January 7, 2005By: Belinda Lee
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Registration No.: 46,863

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Customer No.: 31561
Application No.: 10/605,661
Docket No.: 11314-US-PA

AMENDMENTS

In The Claims

1. (original) A thin film transistor, comprising:
a gate electrode, formed on a substrate, wherein the gate electrode has at least one notch;
a gate dielectric layer, formed over the substrate, covering the gate electrode;
a source region, formed on the gate dielectric layer, wherein the source region is located over a region outside the notch of the gate electrode and the source region overlaps a portion of the gate electrode;
a drain region, formed over the gate dielectric layer exposed by the source region, wherein the drain region is over the notch of the gate electrode and the drain region overlaps a portion of the gate electrode at the edge of the notch; and
a channel layer formed on the gate dielectric layer and located over the gate electrode and between the source region and drain region.
2. (original) The thin film transistor of claim 1, further comprising an etch stop layer formed between the channel layer and the source and drain regions.
3. (original) The thin film transistor of claim 1, further comprising an ohmic-contact layer formed between the channel layer and the source and drain regions.
4. (original) The thin film transistor of claim 1, wherein the source region overlaps the gate electrode.

Customer No.: 31561
Application No.: 10/605,661
Docket No.: 11314-US-PA

5. (original) The thin film transistor of claim 1, wherein the source region comprises two strip regions, each of the two strip regions adjacent to each longitude of the drain region.

6. (original) The thin film transistor of claim 1, wherein the shape of the notch of the gate electrode is a triangle, a quadrilateral or a non-regular shape.

7. (original) A pixel structure, comprising:

a scan line, formed on a substrate;

a gate electrode, formed on the substrate and electrically connected to the scan line, wherein the gate electrode has at least one notch;

a gate dielectric layer, formed over the substrate, covering the scan line and the gate electrode;

a channel layer, formed over the gate dielectric layer and located over the gate electrode;

a source region, formed on the channel layer, wherein the source region is over a region outside the notch of the gate electrode and the source region overlaps a portion of the gate electrode;

a drain region, formed over the channel layer exposed by the source region, wherein the drain region is over the notch of the gate electrode and the drain region overlaps a portion of the gate electrode at the edge of the notch;

a data line, formed on the gate dielectric layer, wherein the data line is electrically connected to the source region;

Customer No.: 31561
Application No.: 10/605,661
Docket No.: 11314-US-PA

a protection layer, formed over the substrate, covering the gate electrode, the gate dielectric layer, the channel layer, the source region, the drain region, the scan line and the data line;

a contact, formed within the protection layer and electrically connected to the drain region; and

a pixel electrode, formed on the protection layer, the pixel electrode electrically connected to the drain region through the contact.

8. (original) The pixel structure of claim 7, further comprising an etch stop layer formed between the channel layer and the source and drain regions.

9. (original) The pixel structure of claim 7, further comprising an ohmic-contact layer formed between the channel layer and the source and drain regions.

10. (original) The pixel structure of claim 7, wherein the source region overlaps the gate electrode.

11. (original) The pixel structure of claim 7, wherein the source region comprises two strip regions, each of the two strip regions adjacent to each longitude of the drain region.

12. (original) The pixel structure of claim 11, wherein the source region further extends over the gate dielectric layer formed on the scan line.

13. (original) The pixel structure of claim 7, wherein the shape of the notch of the gate electrode is a triangle, a quadrilateral or a non-regular shape.

Claims 14 -19 (cancelled)

Customer No.: 31561
Application No.: 10/605,661
Docket No.: 11314-US-PA

REMARKS

Response to 35 U.S.C. 121

The Examiner issued a restriction requirement. According to the Office Action, there are patentably distinct species in the claimed invention and a restriction to one of these species in claims is required under 35 U.S.C. 121.

According to species made by the Office Action, Applicant elects the Species I, specified in claims 1-13. Please cancel claims 14-19 without prejudice, disclaimer or waiver. Applicant also reserves the right to pursue the subject matter of the non-elected claims in a divisional application if Applicants so choose.

Customer No.: 31561
Application No.: 10/605,661
Docket No.: 11314-US-PA

CONCLUSION

In view of the foregoing, claims 1-13 remain pending in the application. Favorable consideration and allowance of the present application and all pending claims are hereby courteously requested. In the event a telephone conversation would expedite the prosecution of this application, the Examiner is encouraged to contact the undersigned attorney to discuss the application.

Respectfully submitted,

Date :

January 7, 2005

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